# [[2, Background: Rel-19 RAN1 proposal (by other companies)]]

Referring to Figure 1, the neural network processing system with tunable probabilistic elements is illustrated. In this aspect, the system is structured to process inputs through various components, beginning with the "Parameters" block that feeds into the "Parameter P-Block" identified as step 1. This block is responsible for managing the parameters necessary for the network's operation. Step 2 shows that the output from the "Parameter P-Block" is directed to the "Neuron P-Block," which processes the inputs labeled as step 3. The interaction between these components is crucial for the overall functionality of the system.Following this, the "Bitwise Multiplication Block," indicated as step 4, receives the processed data, performing multiplication operations essential for neural network computations. Step 5 highlights the "ADDITION Block," which aggregates the results from the multiplication stage. Finally, the outputs are generated and labeled in step 6, culminating the processing sequence.The flow of data through these components illustrates the systematic approach taken in designing the neural network processing system, emphasizing the integration of probabilistic elements to enhance adaptability and robustness in processing capabilities.

# [[3, Background: 2-CW and single-CW receiving]]

The prior solutions include the implementation of reduced complexity MIMO receivers utilizing two receive (Rx) port groups, specifically tailored for scenarios involving two Codewords (2-CW) and single Codeword (single-CW) reception. In cases where the rank exceeds 4, it has been proposed that 2-CW Physical Downlink Shared Channel (PDSCH) transmissions are directed towards each Rx port group, as illustrated in Figure (a). Conversely, for ranks less than or equal to 4, the User Equipment (UE) may employ Log-Likelihood Ratio (LLR) combining derived from the demodulation of both Rx port groups, as depicted in Figure (b). Alternatively, the UE may select a fixed Rx port group or one exhibiting superior Signal-to-Noise Ratio (SNR) for enhanced performance. These approaches aim to optimize the MIMO receiver's functionality while addressing the complexities involved in signal processing and channel management.

# [[4, Background: SRS for antenna switching (xTyR)]]

The prior solutions include the configuration of SRS resource sets specifically designed for antenna switching in xTyR scenarios. In such configurations, a total of \( Q = \frac{y}{x} \) SRS resources is utilized, with each resource comprising \( x \) ports. The \( Q \) SRS resources are transmitted using different symbols through Time Division Multiplexing (TDM). Each of the \( Q \) SRS resources is assigned to distinct User Equipment (UE) antenna ports, ensuring that no two resources share the same port. Historically, \( y \) has been defined as an integer multiple of \( x \), as seen in examples such as 1T2R, 2T4R, 1T4R, 2T6R, and 4T8R. However, it is acknowledged that future developments may explore configurations that do not adhere to this integer-multiple principle, potentially leading to scenarios such as 4T6R and 3T8R.

# [[5, Motivation and issue]]

Aspects of the present disclosure include the exploration of SRS port grouping specifically tailored for foldable devices, focusing on the unique structural challenges posed by their design. The strategic organization of SRS ports may optimize performance in Multiple Input Multiple Output (MIMO) configurations, particularly in the context of foldable phones. The configuration of two receive (Rx) antenna groups, which correspond to the two SRS port groups, may be mounted on the two halves of the foldable device, thereby addressing the limitation that radio frequency (RF) circuitry cannot cross the hinge. This arrangement may facilitate the reduction of MIMO receiver complexity while ensuring effective signal processing and communication capabilities. The implications of antenna switching techniques for various configurations, such as 3T6R and 4T6R, may further enhance MIMO performance. Additionally, the impact of Channel Quality Indicator (CQI) calculations on the overall system performance may be evaluated in relation to these port grouping strategies.

# [[6, Proposal for 3T6R]]

Referring to Figure 2, the Parameter P-Block is a critical component within the neural network processing system, designed to introduce probabilistic elements into the parameters (weights and biases) of the neural network. In this aspect, the block operates by incorporating stochastic mechanisms, such as thermal noise or other random fluctuations, to modify the parameters retrieved from memory. This probabilistic variation enhances the system’s adaptability and robustness.The components of the Parameter P-Block include:1. \*\*DAC (Digital-to-Analog Converter)\*\*: This component converts digital signals into analog voltages (V₁ through Vⱼ) that serve as inputs to the gate of the transistor connected to the fluctuating resistor. It ensures precise control over the modulation process.2. \*\*Fluctuating Resistor\*\*: This element generates controlled random variations in resistance, introducing randomness into the parameters. It utilizes thermal noise or other sources of stochastic behavior to achieve this variability.3. \*\*Vop (Output Voltage)\*\*: This component provides the energy source for the P-Block, driving the operation of the fluctuating resistor and other components.4. \*\*Wij (Output Voltages)\*\*: The resultant output voltages are provided in the form of probabilistic 1’s and 0’s. These probabilistic outputs act as the inputs for the pertinent next stage of the neural network processing system.The workflow of the Parameter P-Block involves processing the parameters (weights and biases) stored in memory through the DAC to obtain precise control signals (V₁ through Vⱼ).

# [[7, Proposal for 4T6R]]

Referring to Figure 2, aspects of the present disclosure include a detailed description of the workflow associated with the Parameter P-Block (200). Parameters, specifically weights and biases, are stored in memory and processed through the Digital-to-Analog Converter (DAC) to obtain precise control signals, denoted as \( V\_1 \) through \( V\_j \). These control signals modulate the gate of the transistor connected to the fluctuating resistor, which introduces probabilistic variations. The modified parameters, represented by the output voltages \( (w\_{ij}) \) in the form of probabilistic 1’s and 0’s, are subsequently utilized in further computational stages of the neural network. This ensures that the parameters carry the desired level of randomness, which is critical for enhancing the adaptability and robustness of the system.

# [[8, Proposal for 3T8R (Alt1)]]

Referring to Figure 3, the Activation P-Block is illustrated, showcasing a system designed to process signals through a series of components. In this aspect, the figure presents a configuration where the input signals \( V\_1, V\_2, \ldots, V\_J \) are directed towards the Digital-to-Analog Converter (DAC) and subsequently processed through fluctuating resistors, represented as \( a\_1, a\_2, \ldots, a\_J \). The output voltage \( V\_{op} \) is influenced by the fluctuating resistor, which is critical for introducing variability in the signal processing. The right side of the figure includes two components: the Stochastic Magnetic Tunnel Junction (401) and the Quantum Tunneling Diode (402), which are pivotal in enhancing the signal processing capabilities through advanced mechanisms.The stochastic element may provide randomness in the processing, while the quantum diode may facilitate efficient signal transmission. This configuration emphasizes the integration of randomness in signal processing, which is essential for improving adaptability and robustness in telecommunications technology.

# [[9, Proposal for 3T8R (Alt2)]]

Referring to Figure 3, the Activation P-Block is an essential component within the neural network processing system, designed to introduce probabilistic elements into input activations. In this aspect, the block operates by incorporating stochastic mechanisms, such as thermal noise or other random fluctuations, to modify the activations received from the previous layer. This probabilistic variation enhances the system’s adaptability and robustness.The components of the Activation P-Block include:1. \*\*DAC (Digital-to-Analog Converter)\*\*: This component converts digital signals into analog voltages (V1 through VJ) that serve as inputs to the gate of the transistor connected to the fluctuating resistor, ensuring precise control over the modulation process.2. \*\*Fluctuating Resistor\*\*: This element generates controlled random variations in resistance, introducing randomness into the activations. It can be implemented using: - \*\*401\*\*: A stochastic magnetic tunnel junction (s-MTJ), as described in the p-bit patent (US10607674B2). - \*\*402\*\*: A quantum tunneling diode that leverages quantum mechanical effects to achieve stochastic behavior.3. \*\*Transistor and Inverter (P-bit Formation)\*\*: The first transistor, the fluctuating resistor, and the subsequent inverter together form a p-bit. This p-bit generates probabilistic outputs, enhancing the neural network’s capability to handle uncertainty and variability in the data.4. \*\*Vop (Output Voltage)\*\*: This component provides the energy source for the Activation P-Block, driving the operation of the fluctuating resistor and other components.5. \*\*ai (Probabilistic Activations)\*\*: The resultant output activations take the form of probabilistic values, which serve as inputs for the next stage of the neural network processing system.

# Extracted Images

Image from Slide 2:

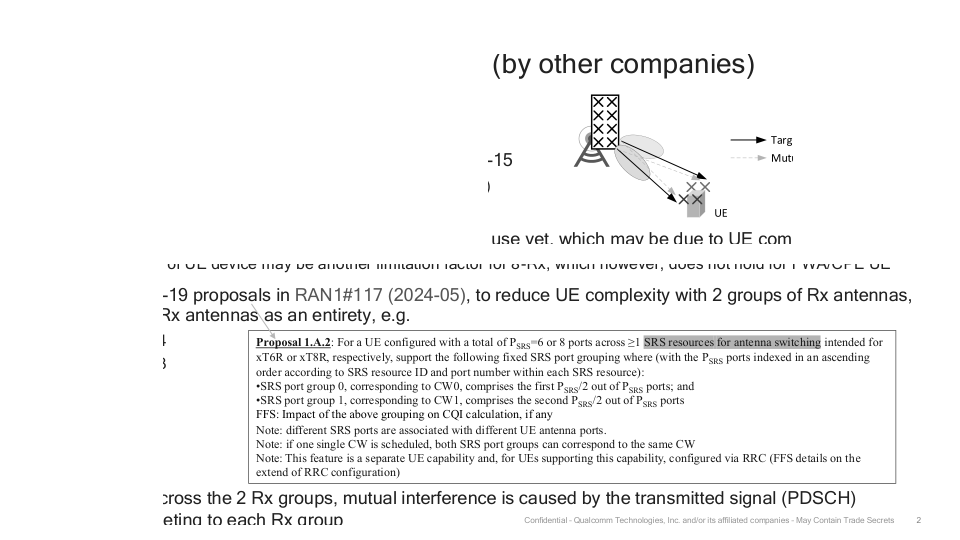


Image from Slide 3:

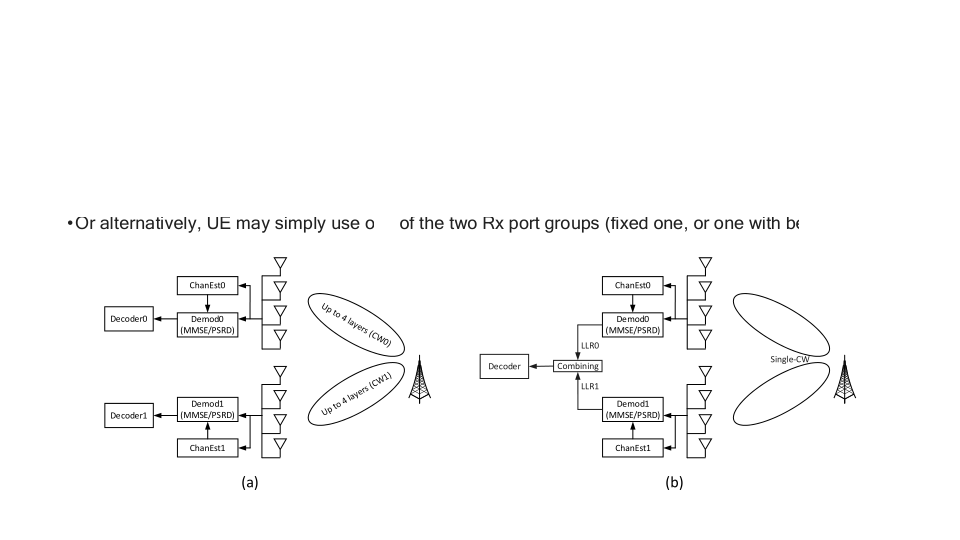


Image from Slide 6:

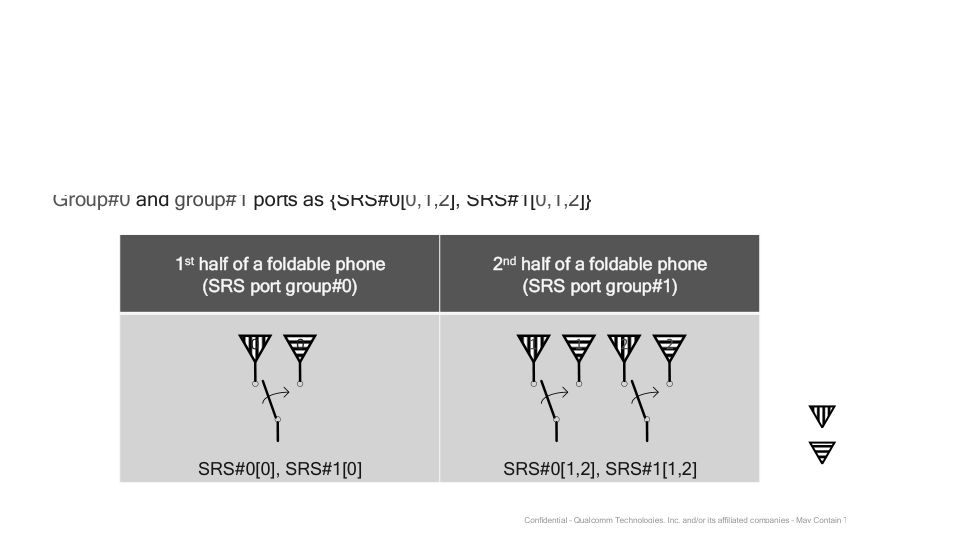


Image from Slide 7:

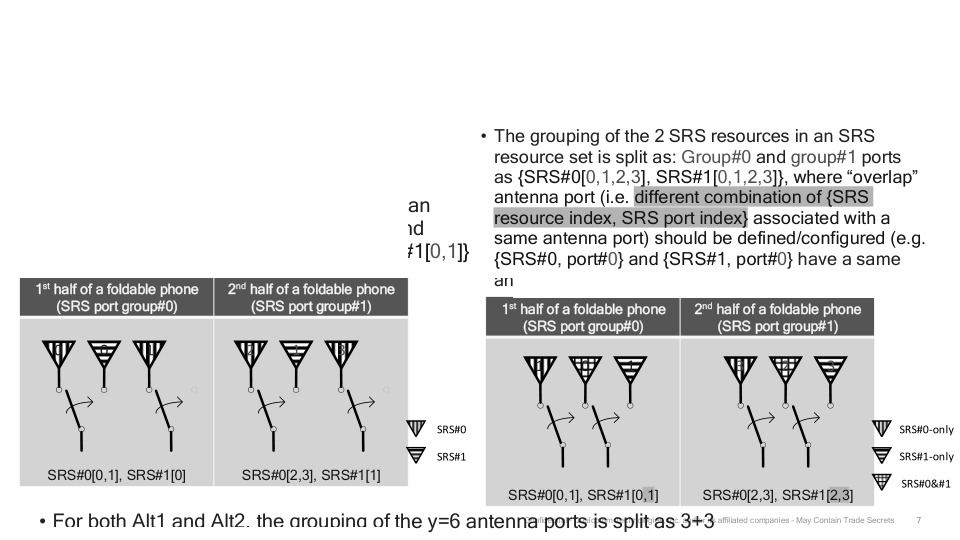


Image from Slide 8:

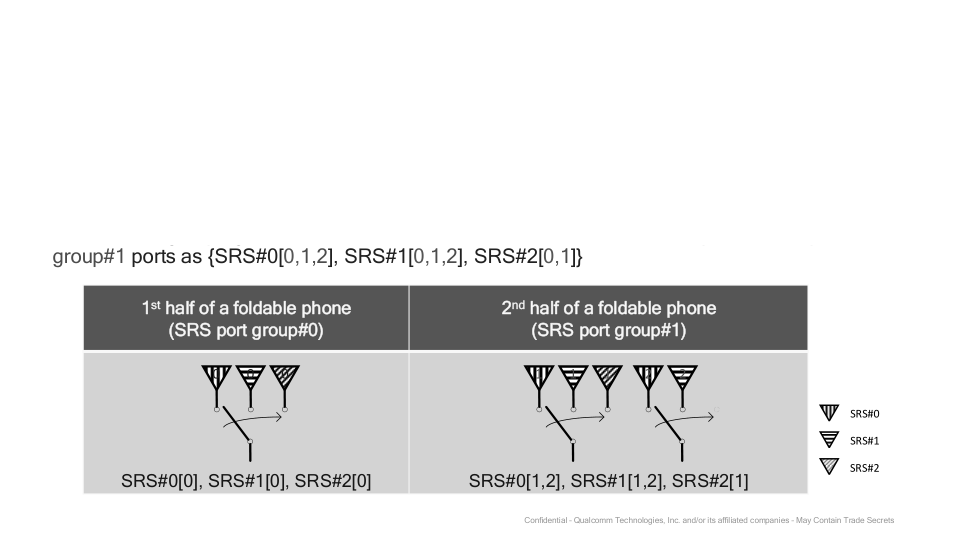
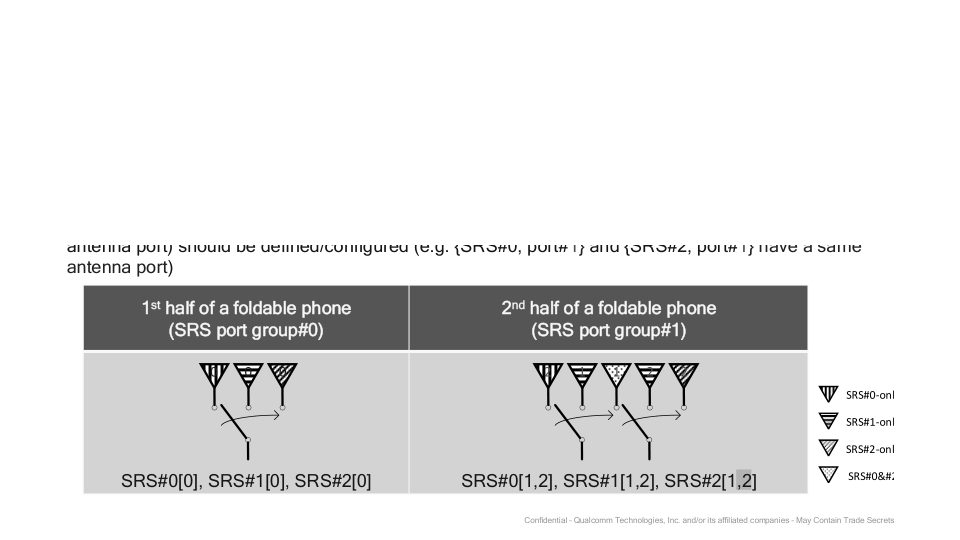


Image from Slide 9:



# Overall Theme

\*\*Theme: "Innovative SRS Port Grouping for Enhanced MIMO Performance in Foldable Devices"\*\*  
  
---  
  
\*\*Key Ideas:\*\*  
1. \*\*SRS Port Grouping\*\*: Focus on the strategic organization of SRS ports to optimize performance in foldable phones.  
2. \*\*MIMO Complexity Reduction\*\*: Addressing the challenges of MIMO receivers through innovative port group configurations.  
3. \*\*Antenna Switching\*\*: Exploring the implications of antenna switching techniques for various configurations (e.g., xT6R, xT8R).  
4. \*\*Foldable Phone Design\*\*: Specific proposals for SRS port configurations tailored to the unique structural challenges of foldable devices.  
5. \*\*CQI Calculation Impact\*\*: Understanding how port grouping affects Channel Quality Indicator calculations.  
6. \*\*RRC Configuration\*\*: Detailing the role of RRC in configuring SRS capabilities for user equipment (UE).  
7. \*\*Neural Network Integration\*\*: Highlighting the incorporation of probabilistic elements in neural networks to enhance adaptability and robustness.  
  
---  
  
\*\*Keywords:\*\*  
- SRS (Sounding Reference Signal)  
- MIMO (Multiple Input Multiple Output)  
- CQI (Channel Quality Indicator)  
- Antenna Switching  
- Foldable Phones  
- RRC (Radio Resource Control)  
- Probabilistic Elements  
- Digital-to-Analog Converter (DAC)  
  
---  
  
\*\*Terminology:\*\*  
- P SRS (Total SRS Ports)  
- CW (Codeword)  
- Rx (Receive)  
- Tx (Transmit)  
- LLR (Log-Likelihood Ratio)  
- TDM (Time Division Multiplexing)  
- Q (Number of SRS Resources)  
- SNR (Signal-to-Noise Ratio)  
  
---  
  
\*\*Visual Elements:\*\*  
- Diagrams illustrating SRS port group configurations.  
- Flowcharts depicting the processing stages in neural networks with probabilistic elements.  
- Circuit diagrams showcasing the Activation P-Block and its components, emphasizing the integration of randomness in signal processing.  
  
---  
  
\*\*Conclusion:\*\*  
This theme encapsulates the innovative approaches to SRS port grouping aimed at enhancing MIMO performance in foldable devices while also integrating advanced neural network processing methods. It emphasizes the importance of adaptability, robustness, and strategic design in modern telecommunications technology.